Laser-Induced Faults in SRAM Memory Cells: Experimental Results and Simulation-based Analysis

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I. Introduction
   Laser fault injection – mechanism
   SRAM fault injection sensitivity

II. Fault model
   Description & Assumptions

III. Experimental results
   Standalone SRAM / µCTRL RAM

IV. Model-based simulation of laser-induced faults

V. Conclusion and perspectives
I. Introduction

- Laser-induced fault injection – mechanism
  - The inverter case

  Sensitive area: reverse biased PN junction (drain of the off transistor)
  
laser => photocurrent => voltage transient (SET)
Laser-induced fault injection – mechanism

- The inverter case

Sensitive area: reverse biased PN junction (drain of the off transistor)

laser => photocurrent => voltage transient (SET)

I. Introduction
Laser-induced fault injection – mechanism

- The inverter case

Sensitive area: reverse biased PN junction (drain of the off transistor)
laser => photocurrent => voltage transient (SET)
Laser-induced fault injection – mechanism (cont.)

- Single Event Upset in a SRAM cell (5T CSRAM)

敏感区域（数据依赖）
Laser-induced fault injection – mechanism (cont.)

- Single Event Upset in a SRAM cell (5T CSRAM)

![Diagram showing the sensitive area in a SRAM cell](image)

Sensitive area (data dependent)
I. Introduction

- Laser-induced fault injection – mechanism (cont.)
  - Single Event Upset in a SRAM cell (5T CSRAM)

```
0 => 1
1 => 0
```

敏感区域 (数据依赖)
I. Introduction

- Laser-induced fault injection – mechanism (cont.)
  - Single Event Upset in a SRAM cell (5T CSRAM)

![Diagram of a 5T CSRAM SRAM cell showing the sensitive area (data dependent).]
II. Fault model

- **Fault model**
  - Bit-flip
    \[ \forall b \rightarrow b' = \overline{b} \]
    Usually assumed
  - Bit-set / Bit-reset
    \[
    \begin{align*}
    \text{Bit-set} & : & \text{if } b = 0 \rightarrow b' = 1 \\
    & & \text{if } b = 1 \rightarrow b' = 1 \\
    \text{Bit-reset} & : & \text{if } b = 0 \rightarrow b' = 0 \\
    & & \text{if } b = 1 \rightarrow b' = 0
    \end{align*}
    \]
    data dependent
  
  \[ \Rightarrow \text{Permits Safe error attacks} \] (e.g. on the key registers)
  
  \[ \Rightarrow \text{Provides additional information on the handled data} \]
II. Fault model

SRAM fault model

CMOS 0.25µm – layout analysis

SEU sensitive areas:
- data dependent
  - state 1
  - state 0

Laser spot size:

⇒ Consistent with bit-set/reset
II. Fault model

☐ SRAM fault model

CMOS 0.25µm – layout analysis

Laser spot size:

⇒ Consistent with bit-flip

⇒ Combination of the two fault models?
III. Experimental results

- Experimental setup

- Frontside injection
- Wavelength: 1064nm (IR)
- Spot size: 1µm, 5µm
- Pulse width: 50ns, 30ps
- Power: 0.26W, 0.42W
- Scan steps: 0.2µm

- SRAM 5T
- CMOS 0.25µm (test chip)
Fault injection sensitivity map

SRAM 5T 0.25\textmu m \ Ø1\textmu m

- no overlap between bit-set and bit-reset areas

⇒ no bit-flips!
III. Experimental results

- Fault injection sensitivity map
  - 8-bit µCTRL
  - CMOS 0.35µm
  - target: RAM memory
  - 6T SRAM cells
III. Experimental results

- Fault injection sensitivity map of μCTRL RAM
  - Laser: $\varnothing$ 1µm / 0.29W / 50ns

$\Rightarrow$ fault model: bit-set/reset (no overlap)
III. Experimental results

Fault injection sensitivity map  \( \mu \text{CTRL RAM} \)

- Laser: \( \varnothing \ 5\mu m / 0.29W / 50\text{ns} \)

\[ \Rightarrow \text{fault model: bit-set/reset} \quad \text{(no overlap)} \]
III. Experimental results

- **Fault sensitivity map (cont.)**
  - PicoseCONDS range laser source
    - pulse duration: 30ps
    - energy: 26nJ

=> fault model: bit-set/reset
IV. Model-based simulation of laser-induced faults

- Electrical modeling of photocurrents induced in PN junctions

Sarafianos et al., *Electrical modeling of the photoelectric effect induced by a pulsed laser applied to an SRAM cell*, Microelectronic Reliability
IV. Model-based simulation of laser-induced faults

Electrical modeling of photocurrents induced in PN junctions

\[ I_{ph} = (a \times V + b) \times S \times \alpha_{gauss} \times V_{laser\_trig} \]

\[ a = p \times P_{laser}^2 + q \times P_{laser} + r \]
\[ b = s \times P_{laser} \]

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>N+/Psub</th>
<th>P+/Nwell</th>
<th>Nwell/Psub</th>
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<tr>
<td>( P )</td>
<td>4E^{-9}</td>
<td>9E^{-5}</td>
<td>6E^{-11}</td>
</tr>
<tr>
<td>( Q )</td>
<td>-5E^{-7}</td>
<td>2E^{-4}</td>
<td>9E^{-9}</td>
</tr>
<tr>
<td>( R )</td>
<td>9E^{-6}</td>
<td>-5E^{-6}</td>
<td>1E^{-7}</td>
</tr>
<tr>
<td>( S )</td>
<td>4E^{-6}</td>
<td>1.2E^{-3}</td>
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</table>

\[ \alpha_{gauss}(d) = \left[ \beta \times \exp\left(-\frac{d^2}{c_1}\right) + \gamma \times \exp\left(-\frac{d^2}{c_2}\right) \right] \times w \]

Sarafianos et al., *Electrical modeling of the photoelectric effect induced by a pulsed laser applied to an SRAM cell*, Microelectronic Reliability
IV. Model-based simulation of laser-induced faults

- Simulation-based SEU sensitivity map of an SRAM

⇒ bit-set/reset fault model confirmed
⇒ qualitative results (model developed for 90nm)
IV. Model-based simulation of laser-induced faults

- Simulation-based SEU sensitivity map of an SRAM
  - Voltages and currents analysis explain the absence of bit-flips
V. Conclusion

- **SRAM fault model**
  - Laser injection

  The relevant fault model is *bit-set/reset* $\emptyset 1-5\mu m / 30\text{ps}-50\text{ns}$

  On exp. and simulation basis

  Only a few bit-flips ($<1\%$) on $\mu$CTRL

- **Perspectives**
  - More exp. tests (technologies, laser parameters)
  - Extend laser effect modelization to picoseconds range
  - Study of registers’ fault model similar or not?
  - Consequences on DFA schemes
Thank you for your attention

Laser benches open for academics on cooperation basis
Bring and test your own device
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