Sensitivity Tuning of a Bulk Built-In Current Sensor for Optimal Transient-Fault Detection

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I. Introduction
   Single Event Effect mechanism
   Bulk Built-In Current Sensor principle

II. Previous BBICS designs
   Limitations

III. Improved BBICS architecture
   Design principles and obtained results

IV. Conclusion and perspectives
I. Introduction

- Integrated circuits in radioactive environment
  - Suffer from various types of Single Event Effects (SEE)
    - Single Event Transient (SET),
    - Single Event Upset (SEU),
    - Single Event Latchup (destructive)
    - Single Event Gate Rupture, etc.

- Bulk Built-In Current Sensor (BBICS)
  - Design to monitor the advent of SETs and SEUs
  - Not to prevent their effects
I. Introduction

- SET mechanism - The inverter case

- SEE current through substrate and well biasing TAPs
I. Introduction

- **SET mechanism - The inverter case**

  - **ionizing ion track**
  - **in ‘1’**
  - **out ‘0’**

  ![Diagram showing inverter case with ionizing ion track](image)

- **SEE current through substrate and well biasing TAPs**
I. Introduction

- **SET mechanism - The inverter case**

- **SEE current through substrate and well biasing TAPs**
I. Introduction

- **SET mechanism - The inverter case**

  ![Diagram of a CMOS inverter with an ionizing ion track](image)

  - **ionizing ion track**
  - **P substrate**
  - **N well**
  - **NMOS**
  - **PMOS**
  - **NTAP**
  - **Metal 1**
  - **MOS gate**

- **SEE current through substrate and well biasing TAPs**
SET mechanism - The inverter case

- SEE current through substrate and well biasing TAPs
I. Introduction

- **BBICS principle**

The diagram illustrates a BBICS (BiCMOS Bipolar Integrated Circuit System) principle with a focus on the PN junction and its connection to Gnd and Vdd. The circuit includes NMOS transistors and a sensitive PN junction within the N well.
I. Introduction

- **BBICS principle**

![Diagram of BBICS principle]

- **P substrate**
- **N well**
- **P+**
- **N+**
- **NMOS**
- **NTAP**
- **Sensitive PN junction**
- **Gnd**

**Diagram Description:**
- The diagram illustrates the BBICS principle with labeled components: P substrate, N well, P+, N+, NMOS, NTAP, and sensitive PN junction. The connections to and from Gnd (ground) are also indicated. The state '0' and '1' are marked with arrows indicating the flow direction.
I. Introduction

- BBICS principle

Diagram showing BBICS principle with NMOS and PMOS transistors, and connections to ground (Gnd) and power supply (Vdd).
I. Introduction

- **BBICS principle**

  - Ionizing ion track
  - PMOS bulk
  - N well
  - NTAP
  - Sensitive PN junction
  - NMOS
  - BBICS
  - P+ to Gnd
  - N+ to Vdd

  - \( P \) substrate
  - \( N \) well

  - Circuit diagram showing the BBICS principle.
I. Introduction

**BBICS principle**

- BBICS: monitor SEE current through node PMOS_bulk

![Diagram showing BBICS principle](image-url)
II. Previous BBICS designs

- Tbulk BICS - Neto et al. 2007 (IEEE Tran. on Nuclear Science)
II. Previous BBICS designs

Mar1k BICS

Alarm triggered

PMOS_bulk = Vdd

Reset
II. Previous BBICS designs

- **Tbulk BICS**
  - Design in 32-nm CMOS predictive technology
  - Suffer from high static power consumption:
    - transistors M9-M10-M11 always ON
    - competition between M1 and M2 currents
  - **Overheads (vs unprotected IC):**

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<tr>
<td>Area overhead</td>
<td>+55%</td>
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<tr>
<td>Power consumption overhead</td>
<td>+100%</td>
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II. Previous BBICS designs

- **Low power BBICS with sleep mode** *(ESREF 2012)*
  - Design in 32-nm CMOS predictive technology
II. Previous BBICS designs

- Low power BBICS with sleep mode (ESREF 2012)
  - Design in 32-nm CMOS predictive technology

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<tr>
<td>Area overhead</td>
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<tr>
<td>Power consumption overhead</td>
<td>+40%</td>
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<tr>
<td>Power consump. Sleep-mode</td>
<td>+25%</td>
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III. Improved BBICS architecture

- Design of a test chip: CMOS 65-nm
  - SET sensitivity threshold
    Defined for an inverter chain of minimal size:
    - PMOS: \( I_{PMOS\_bulk} \) of 50ps@130\( \mu \)A
    - NMOS: \( I_{NMOS\_bulk} \) of 50ps@99\( \mu \)A
  - BBICS sensitivity threshold
    \( I_{PMOS\_bulk} \) duration and amplitude to trigger the alarm
    Has to be lower than the SET sensitivity threshold!
III. Improved BBICS architecture

- Low power BBICS with sleep mode

![Graphs showing current and voltage over time with labels for Ipmos_bulk, Ids_M1, Ids_M2, Flag_b, and Flag.]

- 99.9 to 100 time (ns)
- 0 to 100 current (µA)
- 0 to 1.0 voltage (V)

Failed to detect SET
III. Improved BBICS architecture

- Improved BBICS architecture
  - Asymmetry of the core latch (enhanced detection threshold)
  - Use of Low Vt and High Vt transistors (LVT/HVT):
    - LVT $\Rightarrow$ switch OFF to ON more easily
    - higher current capability
    - HVT $\Rightarrow$ switch OFF to ON less easily
    - lower current capability
  - Appropriate timing of access transistors
    - To avoid competition effect between M1 and M2
III. Improved BBICS architecture

- Improved BBICS architecture

![Diagram of Improved BBICS architecture]

- transient current
- PMOS_bulk = Vdd

- = Gnd
- = Vdd

- M3
- M4
- M7
- M8
- M9
- M1
- M2
- M5
- M6
- M1
- Sleep_mode

Vdd = Vdd
Gnd = Gnd
III. Improved BBICS architecture

- Improved BBICS efficiency

![Graph showing current and voltage changes with time](image)

- $I_{pmos\_bulk}$
- $I_{ds\_M1}$
- $I_{ds\_M2}$
- $Flag$
- $Flag\_b$
- $Flag\_out$
- $gate1$

Alarm triggered on SET

Time (ns): 99.9 to 100.5
III. Improved BBICS architecture

- **Improved BBICS efficiency**

  - **50ps current pulse duration:**

    | # of inverters | 10   | 30   | 50   |
    |----------------|------|------|------|
    | BBICS sensitivity threshold | 76µA | 113µA | 148µA |
    | SET threshold         | 130µA | 133µA | 135µA |

  - **Area overhead:** +30% (including both pBBICS and nBBICS)

  - **Test chip tape out:** October 14th 2013
IV. Conclusion and perspectives

Proposal of an improved BBICS architecture

- Low detection sensitivity thanks to:
  - use of LVT/HVT transistors
  - careful tuning of switching times
- Easier to adapt in various technologies
- On going test chip
IV. Conclusion and perspectives

 Perspectives

- Still room for improvement
  
  A Single Built-in Sensor to Check Pull-up and Pull-down CMOS Networks against Transient Faults, R. Possamai Bastos et al., PATMOS 2013

- Laser testing of the test chip
  
  Picosecond range laser source
Thank you for your attention
Bulk biasing with BBICS in advanced CMOS