Building the electrical model of the pulsed photoelectric laser stimulation of an NMOS transistor in 90nm technology

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Purpose

- Understand the effect of pulsed PLS (Photoelectrical Laser Stimulation) on a diode and then on an NMOS transistor in 90nm technology.

- Present an electrical model of an NMOS transistor under pulsed PLS.
Outline

• Introduction

• Principle of the PLS

• Study of a Psubstrate/N+ junction
  – Diode setup
  – I(V) characteristic
  – Gaussian effect on a PN junction
  – Wafer thickness attenuation
  – Focus dependency
  – Diode modeling

• NMOS transistor
  – Measurement
  – Electrical model
  – Electrical cartographies compared to measures

• Conclusion
Introduction

Failure analysis: extensive use of laser stimulation techniques:
   Expensive and time consuming (≈ 1 day)

This paper presents:

- an electrical model of the pulsed PLS of an NMOS transistor.

Build from: electrical measurements
   (Pulsed Laser equipment)

Goal: Predict the response of an NMOS transistor to PLS in a very small amount of calculation time.
   (≈ 1 mn). → Reduce time on equipment.
Principle of the Continuous Photoelectric Laser Stimulation

Energy of the laser > Energy of the band gap of the silicon

Induced photocurrent

h+/e- separation

P-substrate

SCR

V1=var

V2=gnd
Diode setup
I(V) characteristic

\[ I_{PH} = a.V + b \]

\[ a = f(\text{Plaser}) \]
\[ b = f(\text{Plaser}) \]
Gaussian effect on a PN junction

P-substrate

+a, N

P+

Max Min

Ampere-meter

Current (%)

Distance (µm)

0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9

0 50 100 150 200 250 300
Gaussian like behavior of the N+/P-substrate diode

Characterization made for the three lenses of the Laser equipment (2.5X=1µm – 20X=3.25µm – 100X=13µm).

\[ \alpha_{\text{gauss}}(d) = a \exp\left(-\frac{d^2}{c_1}\right) + b \exp\left(-\frac{d^2}{c_2}\right) \]

\[ I_{PH} = (a \cdot V + b) \cdot \alpha_{gauss} \]
Wafer thickness attenuation

\[ e^{-\alpha z} \]

\[ I_{PH} = (aV + b) \cdot \alpha_{gauss} \cdot Att \]
Focus dependency

$\text{current} = f(z)$

$I_{PH} = (a.V + b) \cdot \alpha_{gauss} \cdot \text{Att.f focus}$
Diode modeling

Voltage controlled current source

\[ I_{PH} = (a \times V + b) \times S \times \alpha_{gauss} \times Att \times f_{ocu} \]

\( S = \text{Area of the PN junction} \)
NMOS Measurement

![NMOS Diagram]

- **Psub**: 0V
- **S**: 0V
- **D**: 1.2V
- **G**: 0V
- **N+**: 0V.6V
- **Loc Psub**: 0V.6V
- **Pulse width**: 20µs

The diagram shows the NMOS structure with specific voltage levels and current flow indicated graphically.
NMOS Modeling & results

Measurement

Electrical simulation
Cartographies
Conclusions

- Electrical simulation of the interaction between laser and silicon on an NMOS transistor in 90nm technology seems to be an extremely reliable, fast and also economical tool.

- The validity of our approach is assessed by the very good correlation obtained between simulations and measurements.

- This work will be extended to PMOS transistors and then more complex gates.
Thank you for your attention…

Q & A