Comparison of Bulk Built-In Current Sensors (BBICS) in terms of Transient-Fault Detection Sensitivity

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Outline

1. Context: transient fault (TF) effects
2. Optimized mitigation solutions
3. Operation mode of a BBICS
4. What is TF detection sensitivity?
5. Comparison of BBICS architectures
6. Conclusions
Tiny systems

Physical limits
Process variability
Low voltage levels
System complexity
High frequencies

ICs more sensitive!
Transient fault effects on ICs

Reliability

Fault Tolerance

Security
Environmental Perturbations

Natural Sources

Artificial Sources

Even at ground level!

Transient Faults
Intentional Perturbations

Good Encryption Results

Faulty Encryption Results

DFA

Transient Faults

Laser

Secret Key

Inputs

Outputs

Input Word
Transient Fault (e.g. SET)

Integrated System

Logic Block 0
Data Register 0
Logic Block 1
Data Register 1
Logic Block 2

Clock

Indirect Soft Error (e.g. SEU)
Transient Fault (e.g. SET)

Integrated System

Logic Block 0 → Data Register 0 → Logic Block 1 → Data Register 1 → Logic Block 2

Direct Soft Error (e.g. SEU)
1. **Nano-systems**
   More sensitive to transient faults

2. **Origin**
   Environmental or intentional sources

3. **Logical effects**
   Indirect or direct soft errors
Contents

② Optimized mitigation solutions
1. **Strategy**
   For mitigation of transient faults

2. **Traditional**
   Detection techniques

3. **BICS**
   Built-In Current Sensors
Mitigation solutions

1. Logic Block
2. Register
3. Clock

Integrated System’s Block

12
Mitigation solutions

Concurrent Error Detection Circuitry

Logic Block → Register

Integrated System’s Block

Concurrent Error Detection Circuitry

fault_flag_signal
Mitigation solutions

Concurrent Error Detection Circuitry

Integrated System’s Block

Logic Block → Register

Clock

Concurrent Error Detection Circuitry

fault_flag_signal

System’s Recovery

or

System’s Restart

or

System’s Deadlock

Alternatives of Actions after Detection
Duplication with Comparison (DWC)
Duplication with Comparison (DWC)
Area overhead > 2x

Duplication with Comparison (DWC)

Time Redundancy (TR)
Area overhead > 2x

High delay degradation

Mitigation solutions

1. Traditional

Duplication with Comparison (DWC)

Logic Block → Data Register → Comparator → Result

Copy of Logic Block → Redundant Register

Clock

Time Redundancy (TR)

Logic Block → Data Register → Comparator → Result

Delay

Redundant Register

Clock

N
Built-In Current Sensor (BICS)

😊 Much smaller than DWC
😊 More efficient than TR

Duplication with Comparison (DWC)

Time Redundancy (TR)
Mitigation solutions

VBICS

BICS at $V_{dd}$ and $V_{ss}$
Mitigation solutions

VBICS

BICS at $V_{DD}$ and $V_{SS}$

FlagP = 0
FlagN = 0
Mitigation solutions

VBICS

BICS at $V_{DD}$ and $V_{SS}$

FlagP = 0

FlagN = 1

Alarm Flag

$1 \rightarrow 0$

$I_{\text{fault}}$
Mitigation solutions

延期退化

delay degradation

检测合法的过渡

detection of legal transitions

延时退化

no delay degradation

检测仅非法的过渡

detection of only illegal transitions

VBICS

<table>
<thead>
<tr>
<th>PMOS-VBICS</th>
<th>FlagP</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS-VBICS</td>
<td>FlagN</td>
</tr>
</tbody>
</table>

BICS at $V_{DD}$ and $V_{SS}$
Mitigation solutions

- Delay degradation
- No delay degradation
- Detection of legal transitions
- Detection of only illegal transitions

**VBICS**

- BICS at $V_{DD}$ and $V_{SS}$

**BBICS**

- BICS at Bulk (body-ties)
1 Strategy
Error detection + Correction Action

2 Traditional
Duplication (+Area); Time Redundancy (+Speed)

3 BICS
VBICS (-Efficiency); BBICS (=Speed, +Efficiency)
Contents

①

②

③ **Operation mode of a BBICS**

④

⑤

⑥


1. **Register**
   Indication of fault

2. **Connections**
   BBICS to monitored gates

3. **Amplification**
   Anomalous transient current
BBICS Operation

1 2 3

Register

LATCH

Flag

Reset
BBICS Operation

1. Connections

Monitored Pull-Up Network

BulkP

Flag

LATCH

Reset
BBICS Operation

Connections

Monitored Pull-Up Network

BulkP

Monitored Pull-Down Network

BulkN

Reset

LATCH

Flag
BBICS Operation

1. Monitored Pull-Down Network
2. Monitored Pull-Up Network
3. Amplification

LATCH

V_{th}

Monitor Pull-Up Network

BulkP

Flag

X_p \cdot W_{min}

X_n \cdot W_{min}

Monitor Pull-Down Network

BulkN
1. **Register**
   Asynchronous latch to memorize fault flag

2. **Connections**
   High-ohmic and pull-up (and -down) transistors

3. **Amplification**
   Transistor sizing: lower Vth, higher detection
What is TF detection sensitivity?
1. Effects of transient faults
2. Threshold of a soft error in a flip-flop
3. Injections: Simulate transient fault currents
Integrated System

Logic Block 0 → Data Register 0 → Logic Block 1 → Data Register 1 → Logic Block 2

Clock → Clock → Clock

Transient Fault

Soft Error
Transient Fault (Masked)

Integrated System

Logic Block 0 → Data Register 0 → Logic Block 1 → Data Register 0 → Logic Block 2

No Soft Error
Profile of Transient Fault

Masked
Profile of Transient Fault

- Masked
- Soft Error
Profile of Transient Fault

Masked  Soft Error  Permanent Effect
What are the smallest profiles of transient faults that cause a soft error?
Profile of Transient Fault

Profile of Transient Fault

Masked

Soft Error

Permanent Effect

What are the smallest profiles of transient faults that cause a soft error?

What is the sensitivity of a memory element in detecting transient faults?
Detection Sensitivity

Clock = 1 GHz
65-nm CMOS
Detection Sensitivity

Flip-Flop

Clock = 1 GHz
65-nm CMOS

Threshold
Detection Sensitivity

To find the smallest $I_{\text{FaultP}}(t)$, resulting in soft error

$I_{\text{FaultP}} = ?$

$t_{\text{Fall}} = ?$

Clock = 1 GHz
65-nm CMOS
Detection Sensitivity

Minimum Detectable Amplitude of Injected Current (µA) vs. Fall Time of Injected Current (ps)

- 1_chain_of_4_inverters_flipflop (PMOS)
Transient fault with $t_{\text{Fall}} = 150$ ps need at least $I_{\text{FaultP}} = 175 \, \mu A$ to cause a soft error.
1 Effects

Masking, soft error, or permanent effect

2 Threshold

Between masking effect and soft error

3 Injections

Curve of minimum currents detectable by flip-flop
Contents

1

2

3

4

5 Comparison of BBICS architectures

6
1 Single
2 Single LVT/HVT
3 Zhang
4 Wirth (Initial)
5 New
6 Modular
Monitored Pull-Up Network

BulkP

FlagP

LATCH

PMOS-BBICS

Reset

HVT

LVT
Monitored Pull-Up Network

Various components labeled with different symbols and connections are shown, including

- LATCH
- PMOS-BBICS
- NMOS-BBICS
- Monitored Pull-Down Network
- FlagP
- FlagN
- BulkP
- BulkN
- HVT
- LVT
Minimum Detectable Amplitude of Injected Current (uA) vs. Fall Time of Injected Current (ps)

- Gray line: 1_chain_of_4_inverters_flipflop (PMOS)
- Red line: 1_chain_of_10_inverters_sbbics (PMOS)
- Green line: 1_chain_of_10_inverters_shsbbics (PMOS)
- Yellow line: 1_chain_of_10_inverters_zbbics (PMOS)
BBICS

Tail Component (LATCH)

Monitored Pull-Down Network

BulkN

Monitored Pull-Up Network

BulkP

New
BBICS

1 2 3 4 5 6

New

Monitored Pull-Up Network

BulkP

PMOS Head

LVT

15·L_{\text{min}}

HVT

Tail Component (LATCH)

NMOS Head

BulkN

15·L_{\text{min}}

Monitored Pull-Down Network
BBICS

1 2 3 4 5 6

New

- Monitored Pull-Up Network
- BulkP
- PMOS Head
- Tail Component (LATCH)
- NMOS Head
- BulkN
- Monitored Pull-Down Network

Upgrading its transient-fault sensitivity
Minimum Detectable Amplitude of Injected Current (uA) vs. Fall Time of Injected Current (ps)

- 1_chain_of_4_inverters_flipflop (PMOS)
- 1_chain_of_10_inverters_sbbics (PMOS)
- 1_chain_of_10_inverters_shsbbics (PMOS)
- 1_chain_of_10_inverters_zbbics (PMOS)
- 1_chain_of_10_inverters_bbics (PMOS)
- 1_chain_of_10_inverters_t1hbbics (PMOS)
Monitored Pull-Up Network

BulkP

PMOS Head

Tail Component (LATCH)

NMOS Head

BulkN

Monitored Pull-Down Network
1. **Single:** the least detection sensitive
2. **Single LVT/HVT:** important feature
3. **Zhang:** inefficient extra feedback transistor
4. **Wirth (Initial):** huge power consumption
5. **New:** the most transient-fault detection sensitive
6. **Modular:** important feature
Contents

1
2
3
4
5
6 Conclusions
Conclusions

1. A simulation method provides a metric
   - Compare the transient-fault detection sensitivity of BBICS architectures
   - Identify BBICS features that produce improvements

2. A new BBICS architecture
   - The best transient-fault detection sensitivity
   - No speed degradation and negligible power consumption overhead

3. Use of LVT and HVT transistors
   - Improve considerably the transient-fault detection sensitivity of BBICS

4. Modular BBICS technique
   - Ensure a competitive area overhead

5. Laser-based test of BBICS chip
   - Validate BBICS approach on CMOS 65-nm
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ionizing ion track

in ‘0’

out ‘1’ => ‘0’

to Gnd

to Vdd

Metal 1

MOS gate

P substrate

N well

PTAP

NMOS

PMOS
The diagram illustrates a circuit with various components labeled as follows:

- **BB CS (Bottom Border Component)**
- **NMOS Bulk**
- **PTAP**
- **Metal 1**
- **MOS Gate**

The connections show:
- **P substrate**
- **N well**

Key connections include:
- **To Gnd**
- **To Vdd**

Additionally, there is a flag labeled **alarm flag** with inputs and outputs indicated as '0' and '1'.
Protection of 10 chains of 10 inverters by one PMOS-BBICS and one NMOS-BBICS (a commercial 65-nm CMOS Technology)